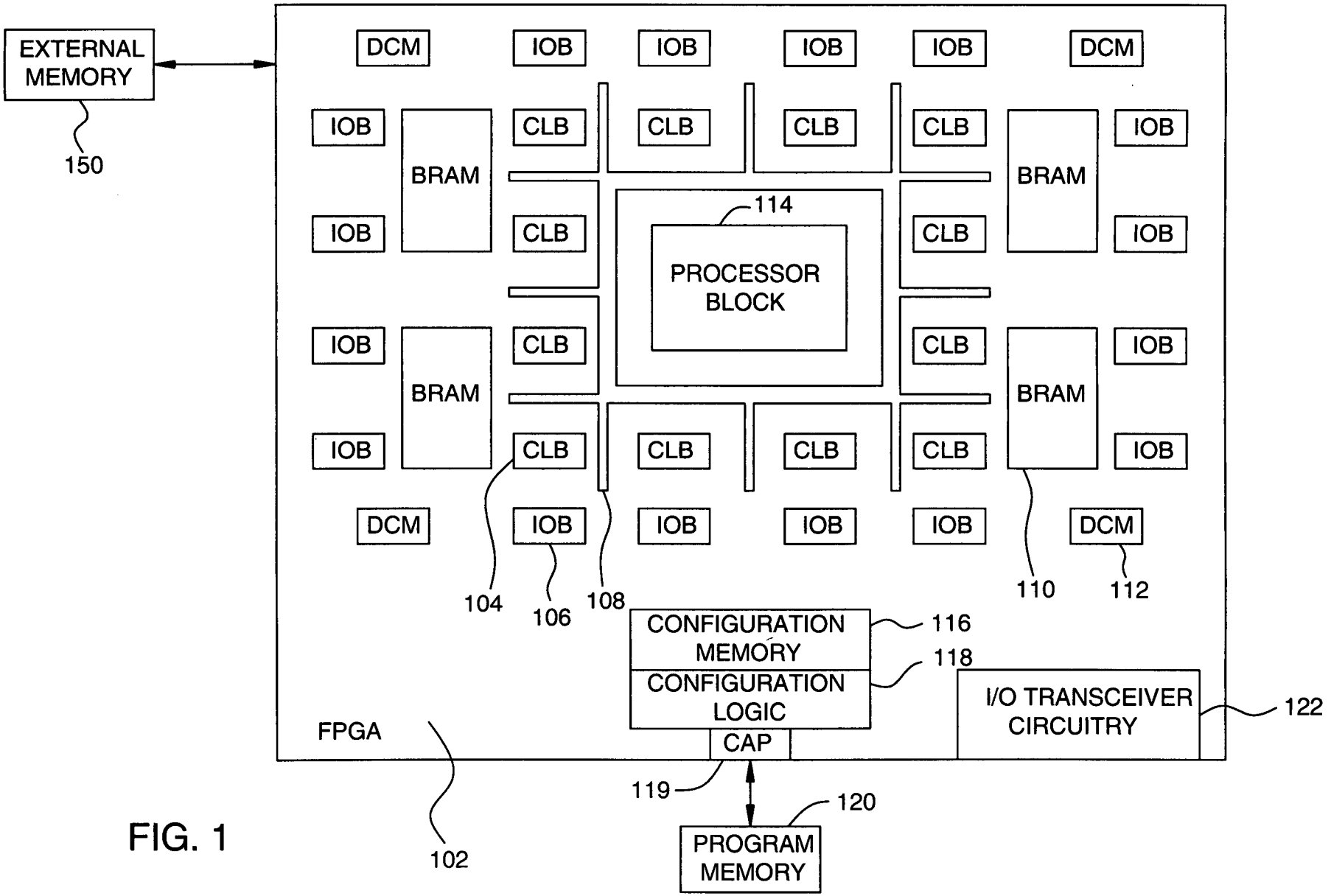

EXTERNAL MEMORY
150
DCM
IOB
IOB
IOB
IOB
DCM
IOB
BRAM
CLB
CLB
CLB
CLB
BRAM
IOB
IOB
CLB
114
PROCESSOR BLOCK
CLB
IOB
IOB
BRAM
CLB
CLB
BRAM
IOB
IOB
CLB
CLB
CLB
CLB
IOB
DCM
IOB
IOB
IOB
IOB
DCM
104
106
108
110
112
CONFIGURATION MEMORY
116
CONFIGURATION LOGIC
118
I/O TRANSCEIVER CIRCUITRY
122
FPGA
CAP
119
120
PROGRAM MEMORY
102

FIG. 1

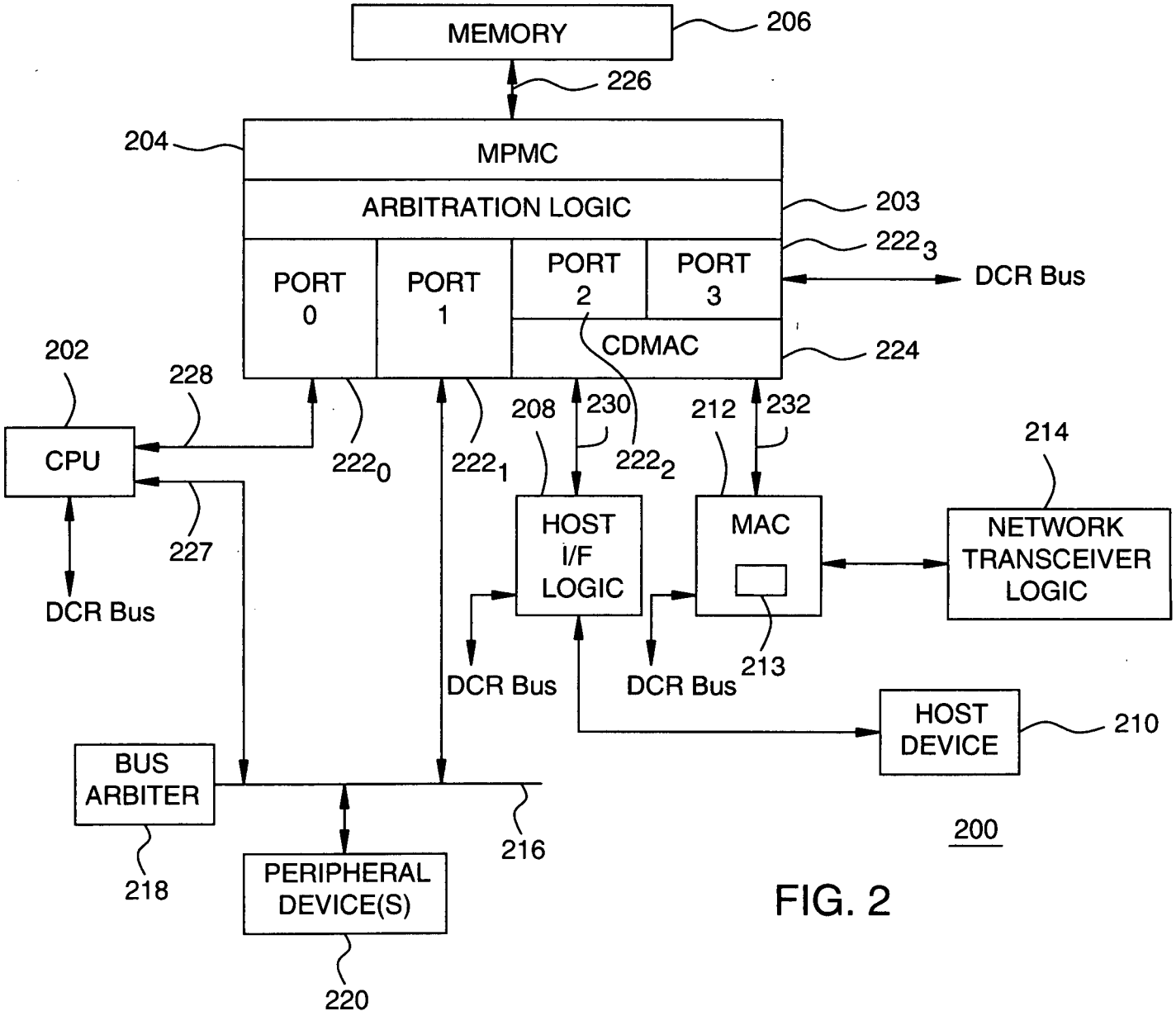

MEMORY
206
226
204
MPMC
ARBITRATION LOGIC
203
PORT 0
PORT 1
PORT 2
PORT 3
222_3
DCR Bus
CDMAC
224
202
228
208
230
212
232
214
CPU
222_0
222_1
222_2
HOST I/F LOGIC
MAC
NETWORK TRANSCEIVER LOGIC
227
DCR Bus
DCR Bus
DCR Bus
213
HOST DEVICE
210
BUS ARBITER
216
218
PERIPHERAL DEVICE(S)
220
200

FIG. 2

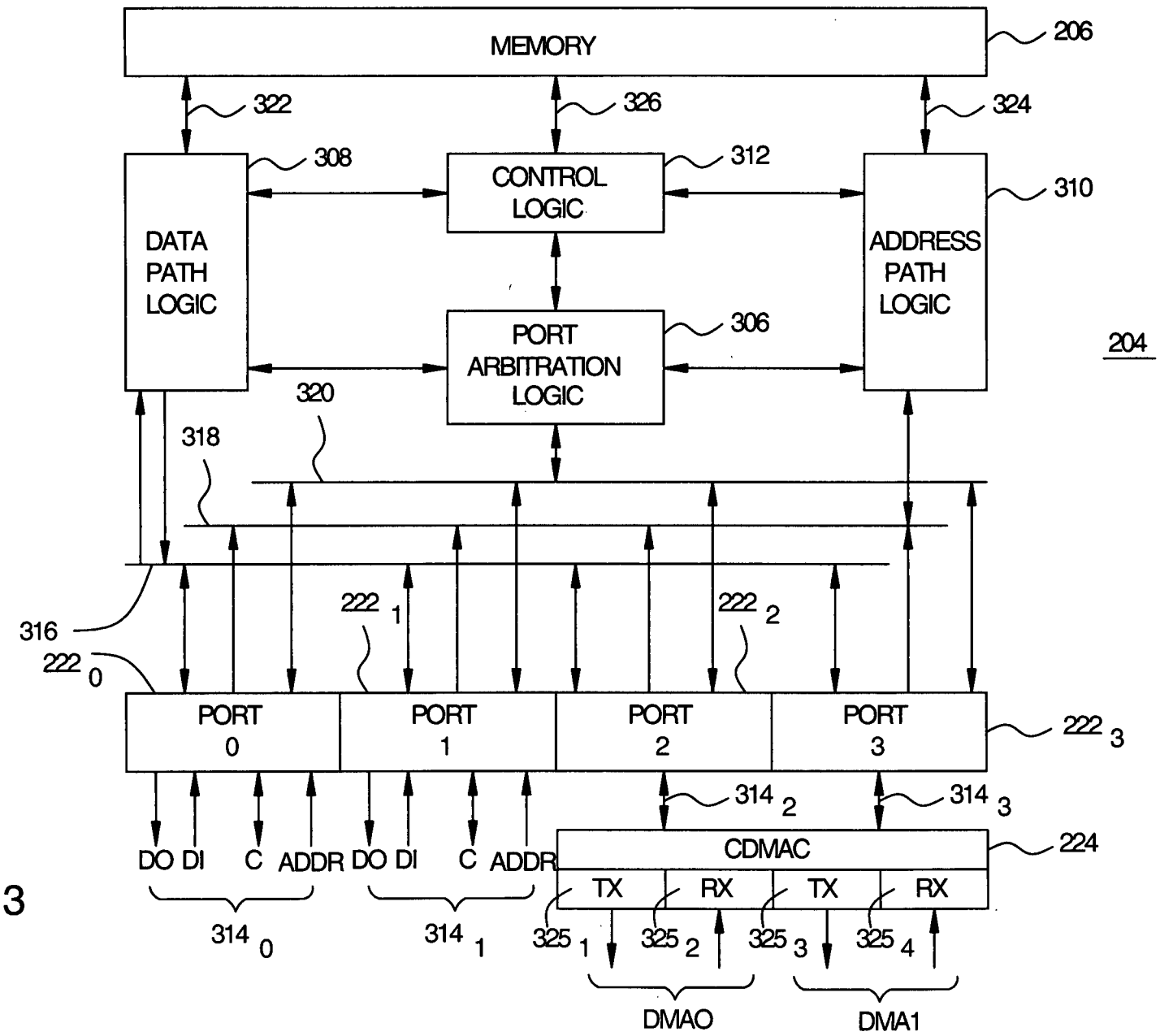
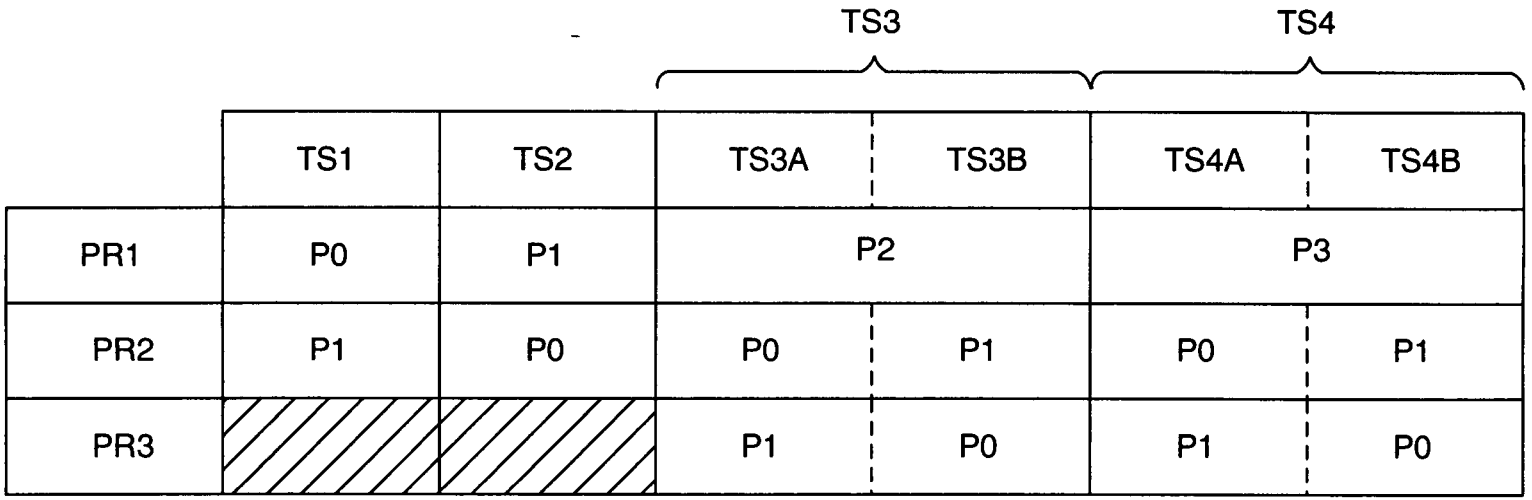

MEMORY
206
322
326
324
308
CONTROL LOGIC
312
DATA PATH LOGIC
310
ADDRESS PATH LOGIC
PORT ARBITRATION LOGIC
306
204
320
318
316
222 0
222 1
222 2
PORT 0
PORT 1
PORT 2
PORT 3
222 3
314 2
314 3
DO DI C ADDR DO DI C ADDR
CDMAC
224
TX RX TX RX
314 0
314 1
325 1
325 2
325 3
325 4
DMAO
DMA1

FIG. 3


TS3
TS4
TS1
TS2
TS3A
TS3B
TS4A
TS4B
PR1
P0
P1
P2
P3
PR2
P1
P0
P0
P1
P0
P1
PR3
P1
P0
P1
P0

400

FIG. 4

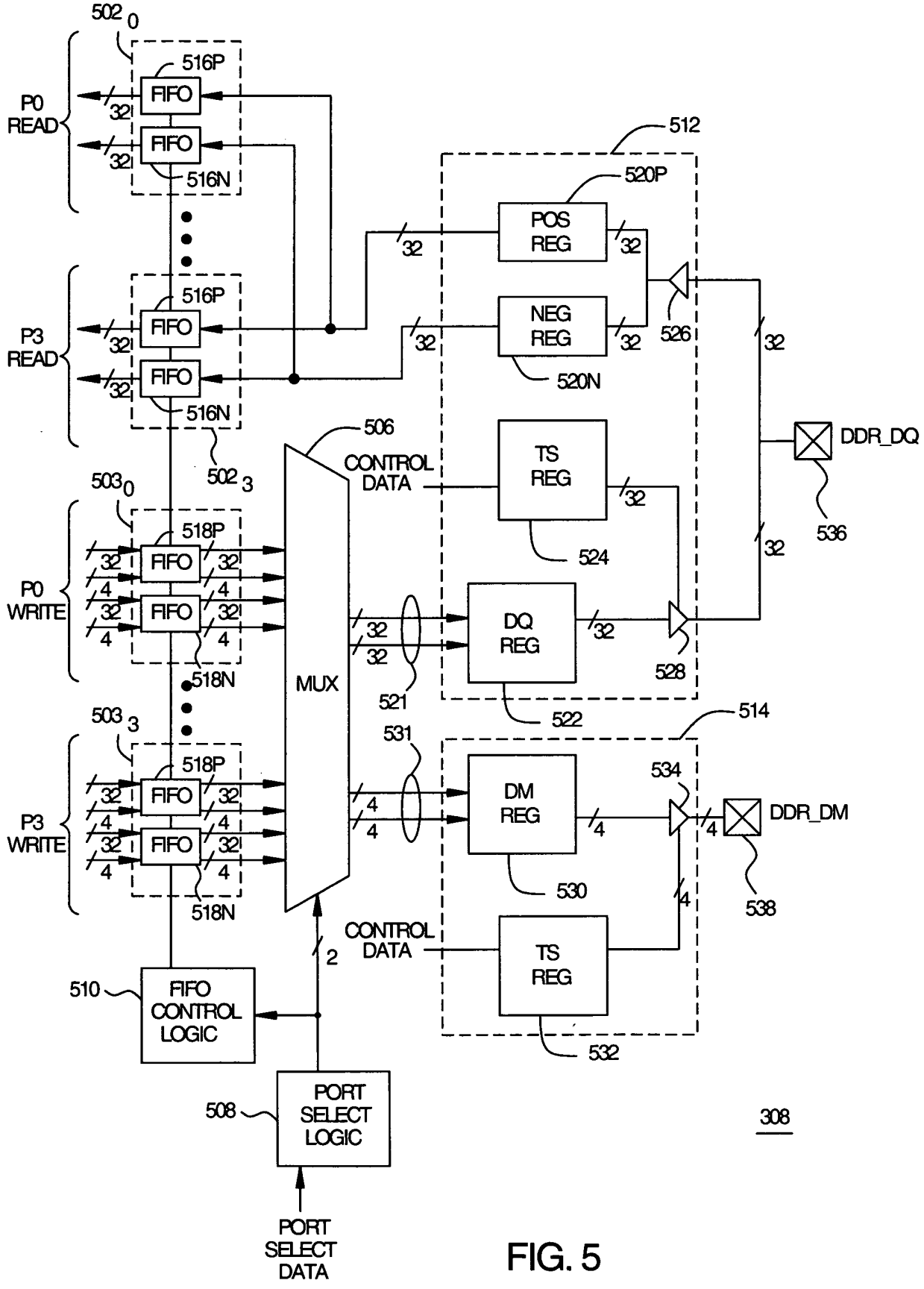

502 0
516P
FIFO
P0 READ
32
FIFO
516N
512
520P
POS REG
32
NEG REG
520N
526
P3 READ
516P
FIFO
FIFO
516N
502 3
506
CONTROL DATA
TS REG
524
DDR_DQ
536
503 0
518P
P0 WRITE
4
518N
MUX
DQ REG
528
521
522
514
503 3
531
P3 WRITE
518P
DM REG
534
DDR_DM
530
538
CONTROL DATA
TS REG
532
510
FIFO CONTROL LOGIC
2
508
PORT SELECT LOGIC
308
PORT SELECT DATA

FIG. 5

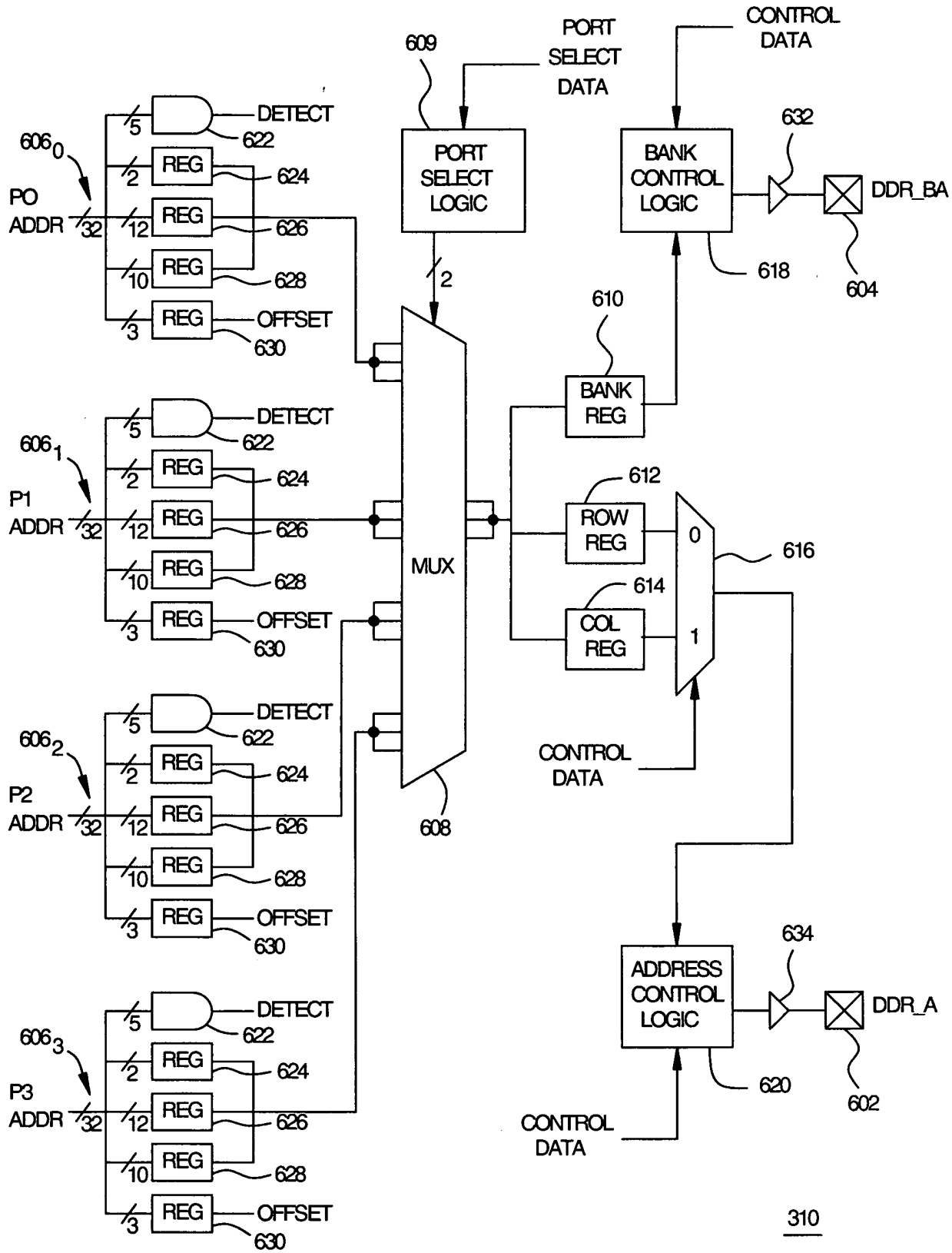

PORT SELECT DATA
609
CONTROL DATA
PORT SELECT LOGIC
BANK CONTROL LOGIC
632
DDR_BA
604
618
610
BANK REG
612
ROW REG
614
COL REG
0
1
616
MUX
608
CONTROL DATA
ADDRESS CONTROL LOGIC
634
DDR_A
602
620
CONTROL DATA
606_0
PO ADDR
606_1
P1 ADDR
606_2
P2 ADDR
606_3
P3 ADDR
DETECT
622
REG
624
626
628
OFFSET
630
310

FIG. 6

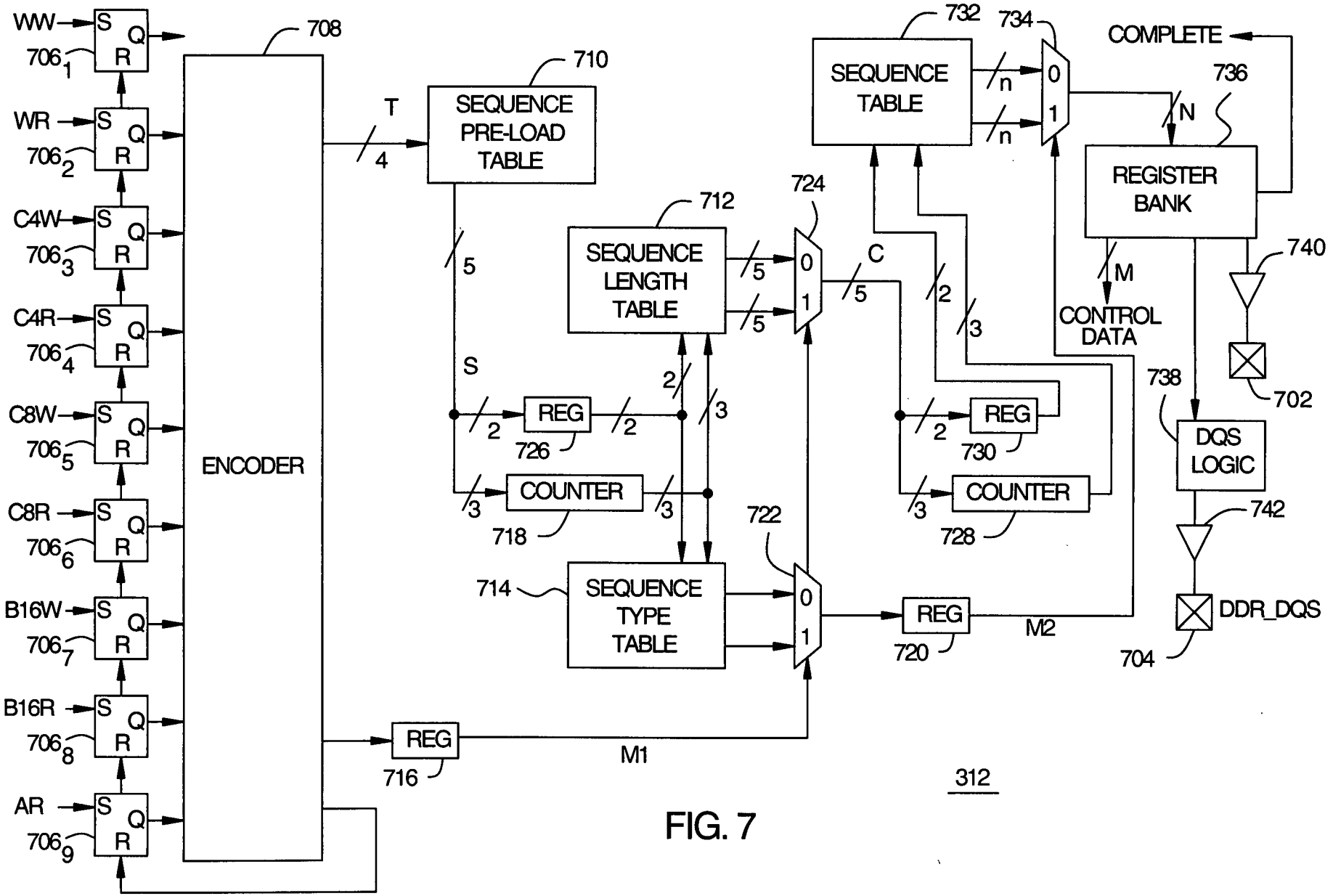

WW
WR
C4W
C4R
C8W
C8R
B16W
B16R
AR
S
Q
R
706 1
706 2
706 3
706 4
706 5
706 6
706 7
706 8
706 9
ENCODER
708
T
4
SEQUENCE PRE-LOAD TABLE
710
5
S
2
REG
726
2
2
3
COUNTER
718
3
3
SEQUENCE LENGTH TABLE
712
5
5
724
0
1
C
5
714
SEQUENCE TYPE TABLE
722
REG
716
M1
SEQUENCE TABLE
732
n
n
734
0
1
COMPLETE
736
N
REGISTER BANK
M
CONTROL DATA
740
702
738
DQS LOGIC
742
DDR_DQS
704
2
REG
730
2
3
COUNTER
728
3
REG
720
M2
312

FIG. 7

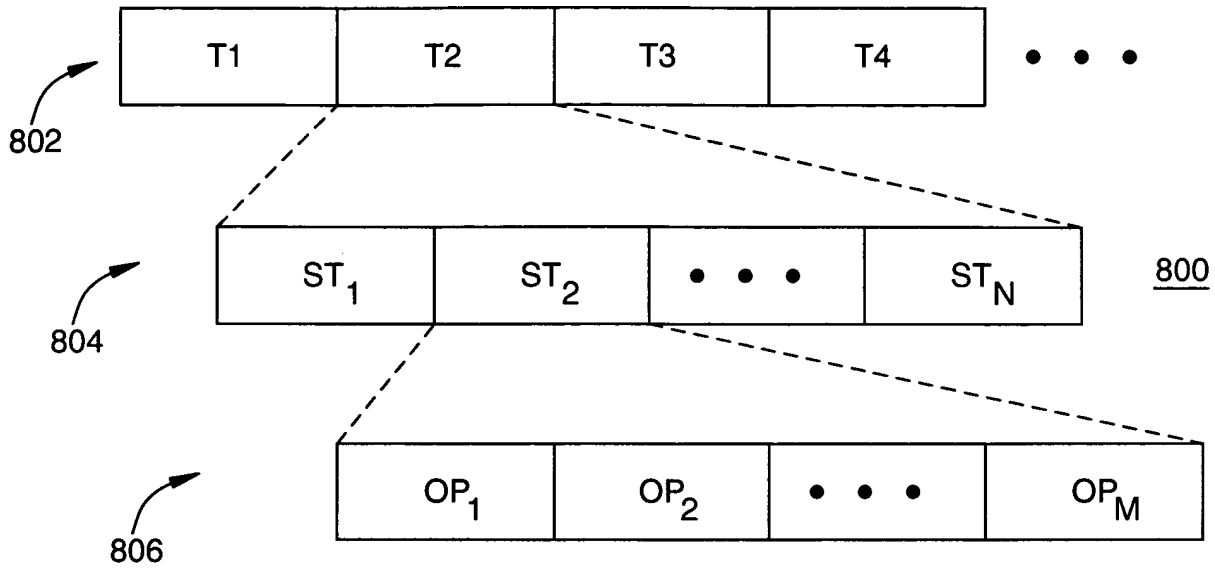

T1
T2
T3
T4
802
ST1
ST2
STN
804
800
OP1
OP2
OPM
806

FIG. 8

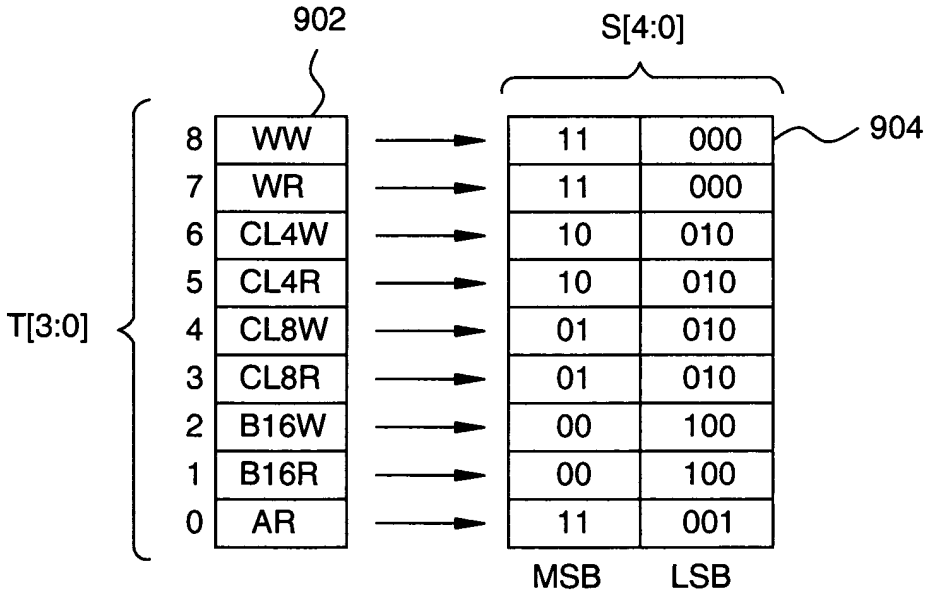

902
S[4:0]
904
T[3:0]
8 WW 11 000
7 WR 11 000
6 CL4W 10 010
5 CL4R 10 010
4 CL8W 01 010
3 CL8R 01 010
2 B16W 00 100
1 B16R 00 100
0 AR 11 001
MSB
LSB

FIG. 9

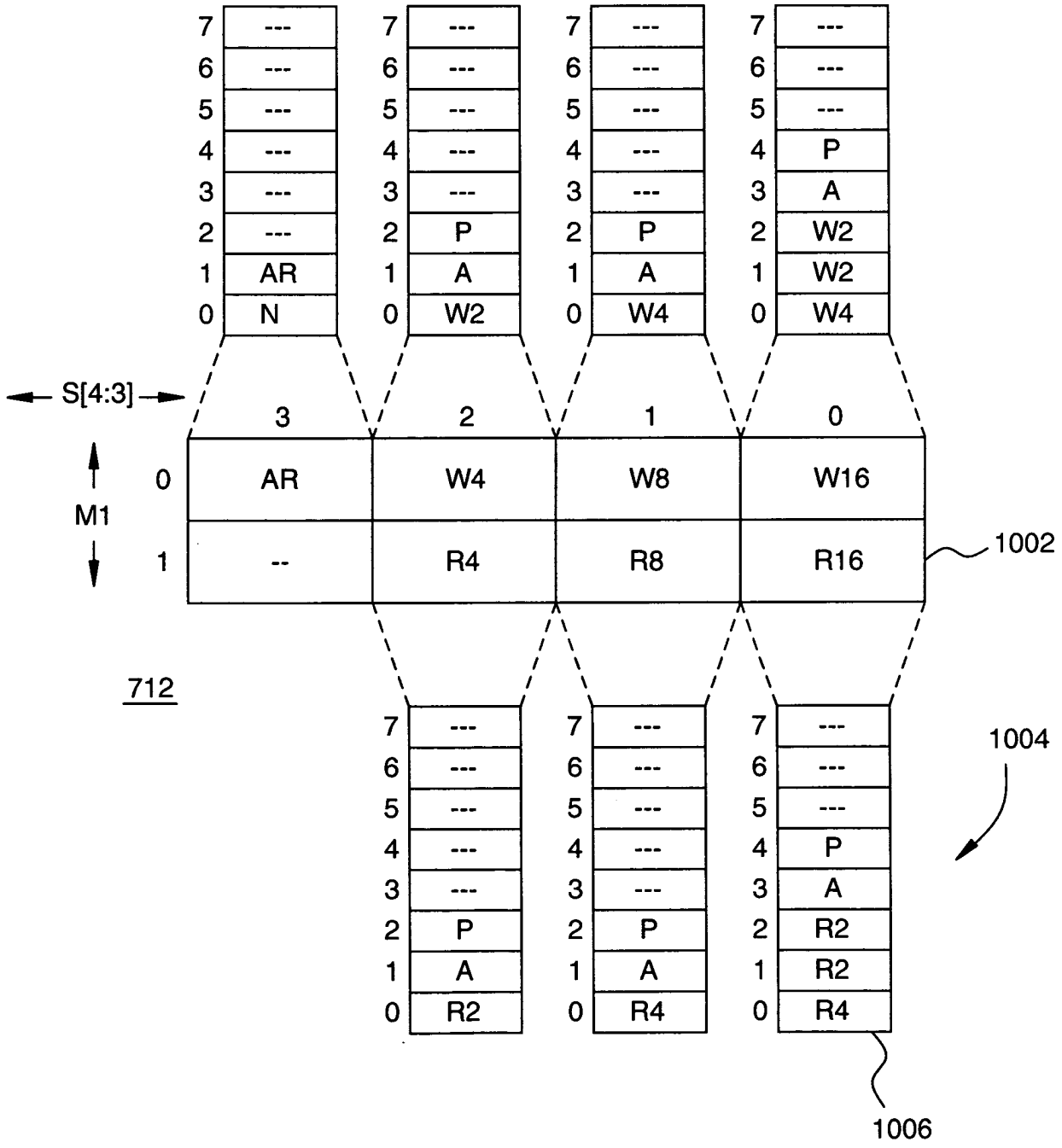

7 --- 6 --- 5 --- 4 --- 3 --- 2 --- 1 AR 0 N
7 --- 6 --- 5 --- 4 --- 3 --- 2 P 1 A 0 W2
7 --- 6 --- 5 --- 4 --- 3 --- 2 P 1 A 0 W4
7 --- 6 --- 5 --- 4 P 3 A 2 W2 1 W2 0 W4
S[4:3]
3 2 1 0
M1
0 AR W4 W8 W16
1 -- R4 R8 R16
1002
712
7 --- 6 --- 5 --- 4 --- 3 --- 2 P 1 A 0 R2
7 --- 6 --- 5 --- 4 --- 3 --- 2 P 1 A 0 R4
7 --- 6 --- 5 --- 4 P 3 A 2 R2 1 R2 0 R4
1004
1006

FIG. 10

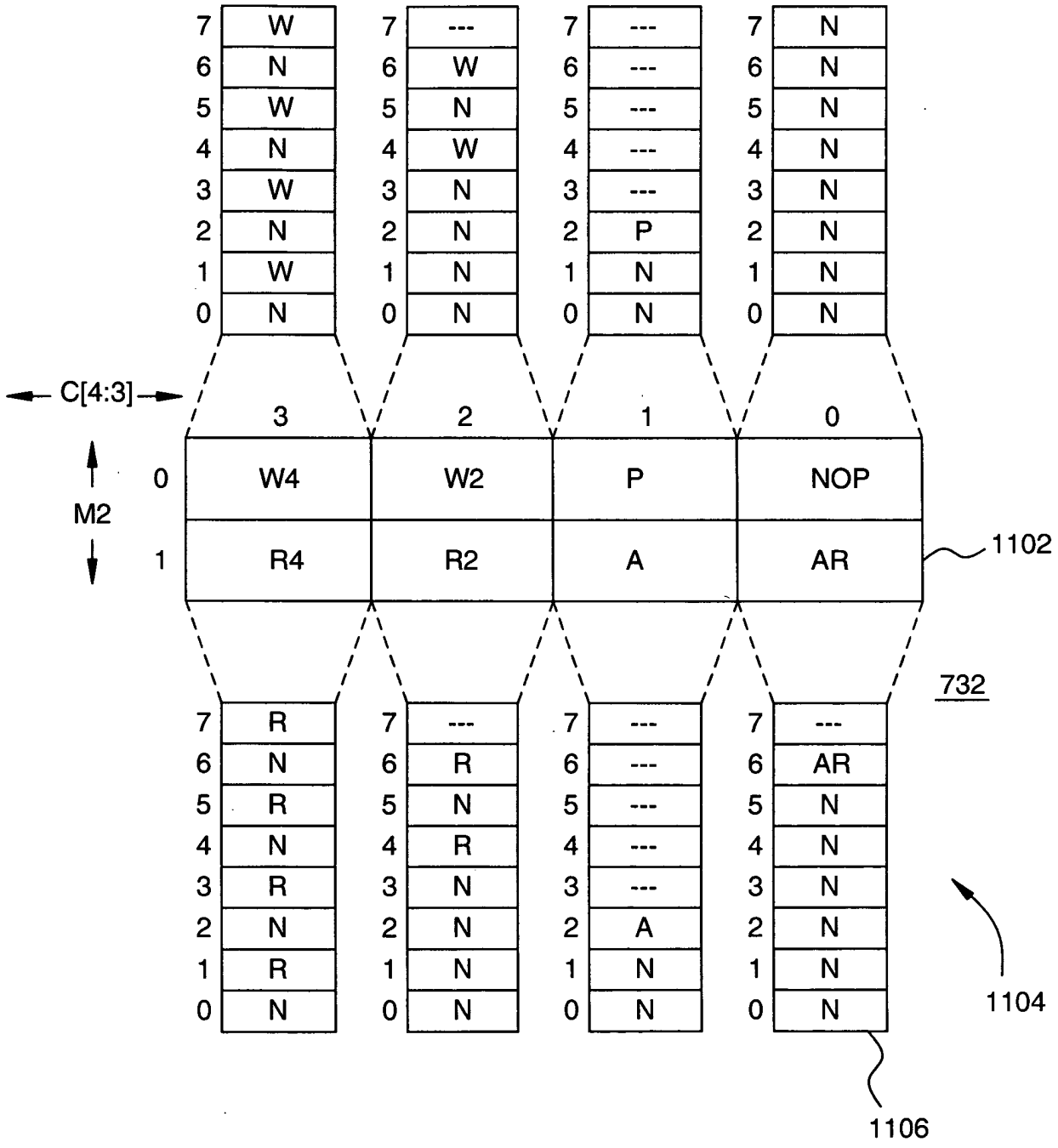

C[4:3]
3
2
1
0
M2
0
1
W4
W2
P
NOP
R4
R2
A
AR
1102
732
1104
1106
7 W 6 N 5 W 4 N 3 W 2 N 1 W 0 N
7 --- 6 W 5 N 4 W 3 N 2 N 1 N 0 N
7 --- 6 --- 5 --- 4 --- 3 --- 2 P 1 N 0 N
7 N 6 N 5 N 4 N 3 N 2 N 1 N 0 N
7 R 6 N 5 R 4 N 3 R 2 N 1 R 0 N
7 --- 6 R 5 N 4 R 3 N 2 N 1 N 0 N
7 --- 6 --- 5 --- 4 --- 3 --- 2 A 1 N 0 N
7 --- 6 AR 5 N 4 N 3 N 2 N 1 N 0 N

FIG. 11

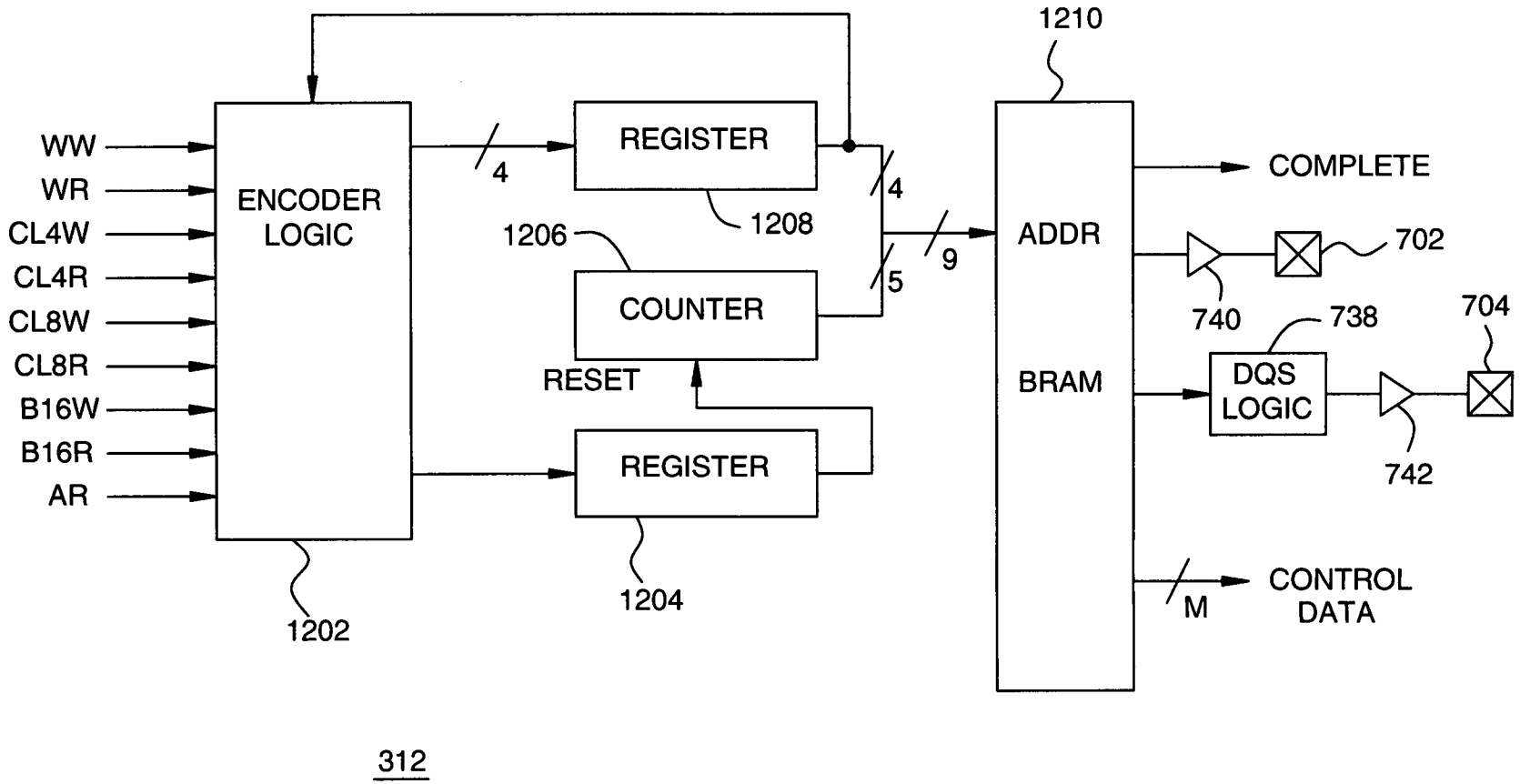

WW
WR
CL4W
CL4R
CL8W
CL8R
B16W
B16R
AR
ENCODER LOGIC
1202
4
REGISTER
1208
1206
COUNTER
RESET
REGISTER
1204
4
5
9
1210
ADDR
BRAM
COMPLETE
702
740
738
704
DQS LOGIC
742
M
CONTROL DATA
312

FIG. 12

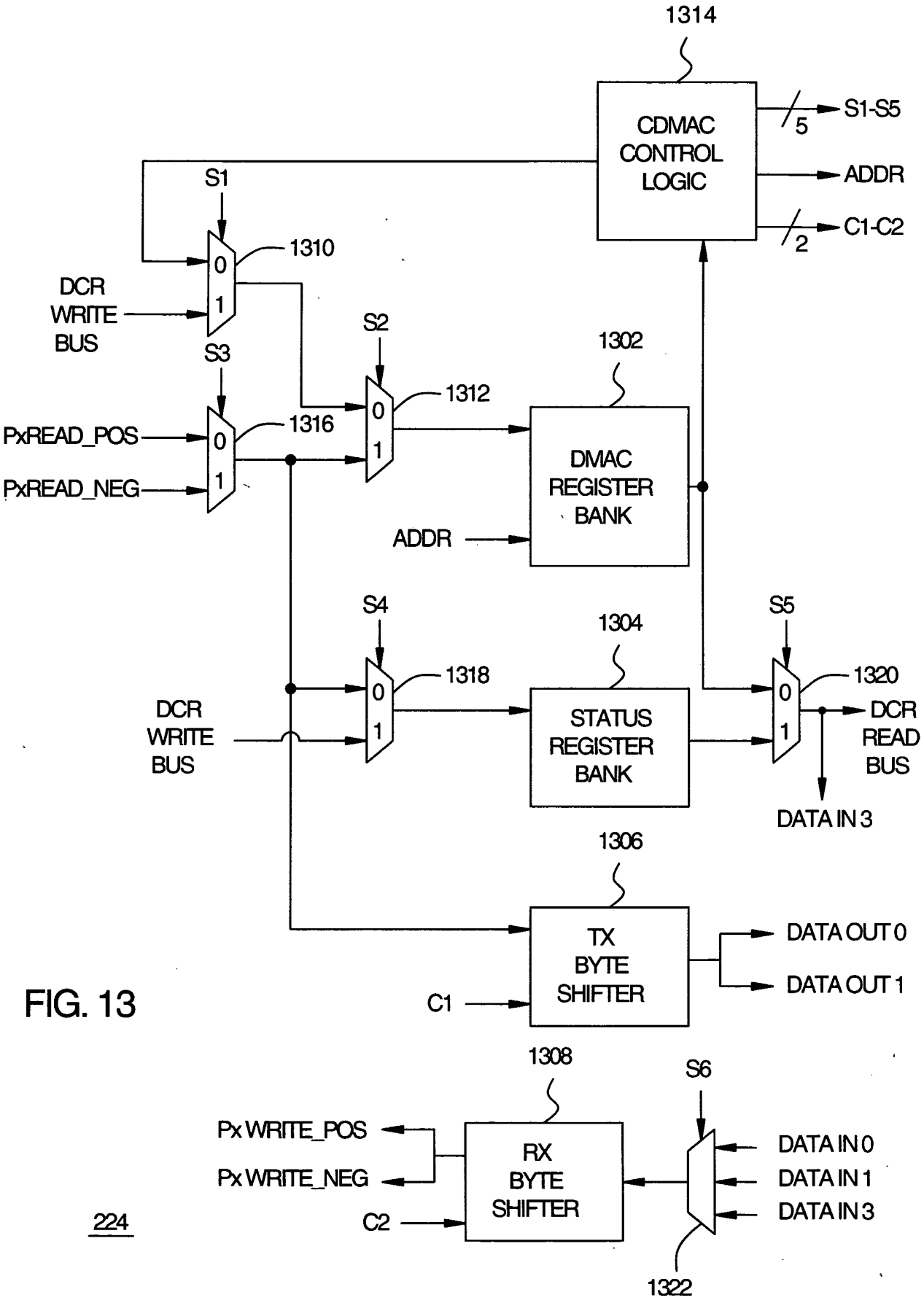

1314
CDMAC CONTROL LOGIC
S1-S5
5
ADDR
C1-C2
2
S1
1310
DCR WRITE BUS
S2
1302
S3
1312
PxREAD_POS
1316
PxREAD_NEG
DMAC REGISTER BANK
ADDR
S4
1304
S5
1318
1320
DCR WRITE BUS
STATUS REGISTER BANK
DCR READ BUS
DATA IN 3
1306
TX BYTE SHIFTER
DATA OUT 0
DATA OUT 1
C1
1308
S6
PxWRITE_POS
PxWRITE_NEG
RX BYTE SHIFTER
DATA IN 0
DATA IN 1
DATA IN 3
C2
224
1322

FIG. 13

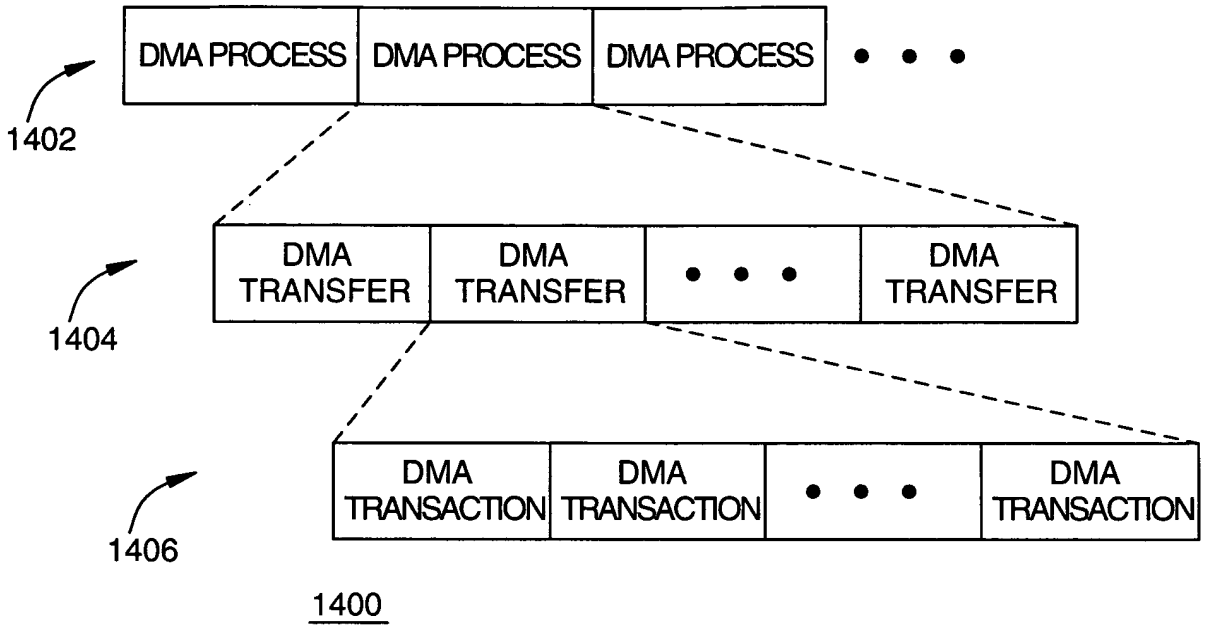

DMA PROCESS
DMA PROCESS
DMA PROCESS
1402
DMA TRANSFER
DMA TRANSFER
DMA TRANSFER
1404
DMA TRANSACTION
DMA TRANSACTION
DMA TRANSACTION
1406
1400

FIG. 14

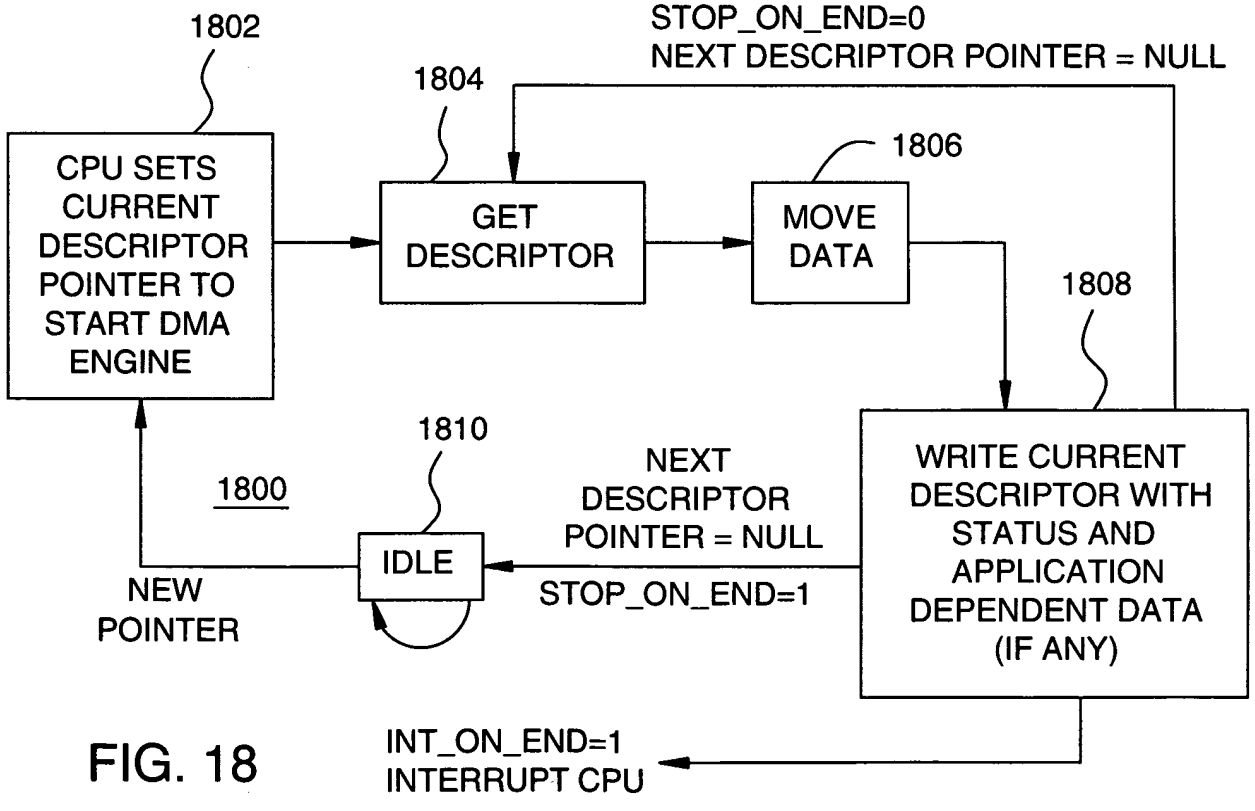

1802
CPU SETS CURRENT DESCRIPTOR POINTER TO START DMA ENGINE
1804
GET DESCRIPTOR
STOP_ON_END=0
NEXT DESCRIPTOR POINTER = NULL
1806
MOVE DATA
1808
WRITE CURRENT DESCRIPTOR WITH STATUS AND APPLICATION DEPENDENT DATA (IF ANY)
1810
IDLE
1800
NEXT DESCRIPTOR POINTER = NULL
STOP_ON_END=1
NEW POINTER
INT_ON_END=1
INTERRUPT CPU

FIG. 18

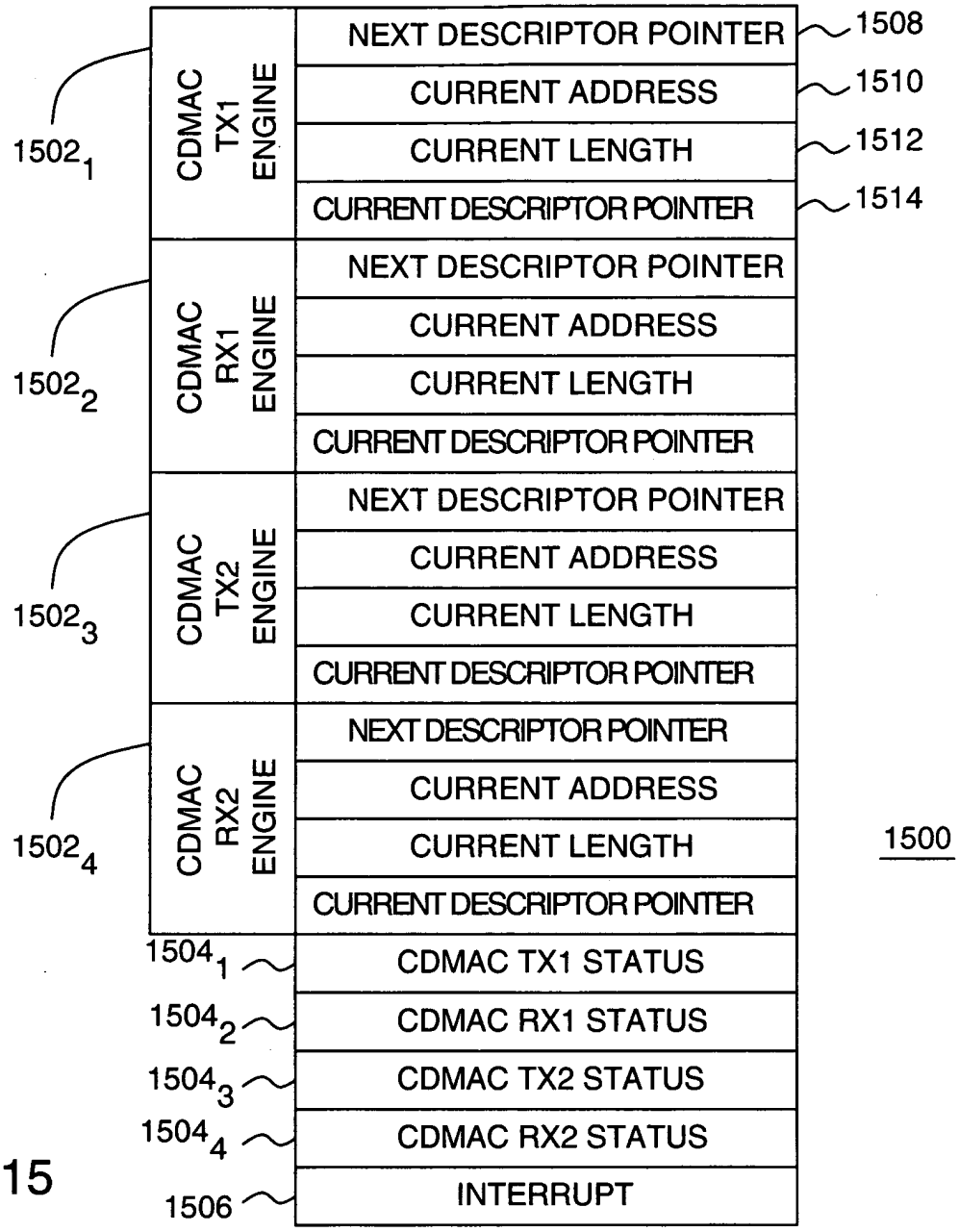

CDMAC TX1 ENGINE
NEXT DESCRIPTOR POINTER
CURRENT ADDRESS
CURRENT LENGTH
CURRENT DESCRIPTOR POINTER
1502 1
1508
1510
1512
1514
CDMAC RX1 ENGINE
NEXT DESCRIPTOR POINTER
CURRENT ADDRESS
CURRENT LENGTH
CURRENT DESCRIPTOR POINTER
1502 2
CDMAC TX2 ENGINE
NEXT DESCRIPTOR POINTER
CURRENT ADDRESS
CURRENT LENGTH
CURRENT DESCRIPTOR POINTER
1502 3
CDMAC RX2 ENGINE
NEXT DESCRIPTOR POINTER
CURRENT ADDRESS
CURRENT LENGTH
CURRENT DESCRIPTOR POINTER
1502 4
1500
1504 1
CDMAC TX1 STATUS
1504 2
CDMAC RX1 STATUS
1504 3
CDMAC TX2 STATUS
1504 4
CDMAC RX2 STATUS
1506
INTERRUPT

FIG. 15

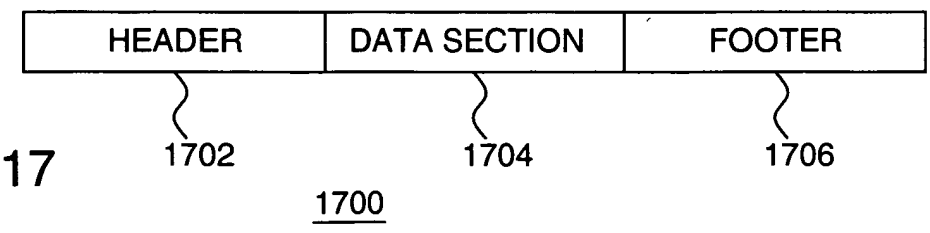

HEADER
DATA SECTION
FOOTER
1702
1704
1706
1700

FIG. 17

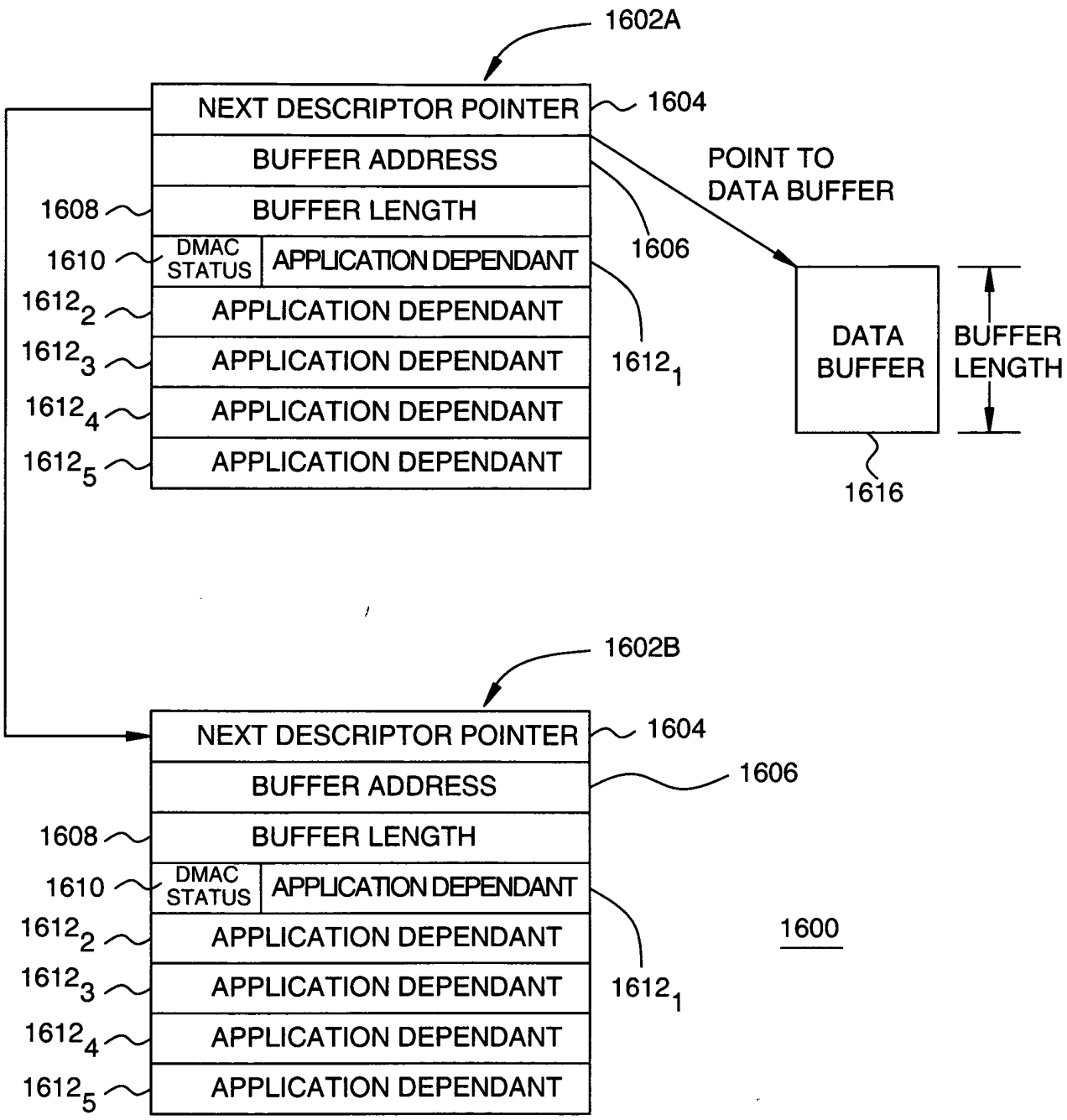

1602A
NEXT DESCRIPTOR POINTER
1604
BUFFER ADDRESS
POINT TO
DATA BUFFER
1608
BUFFER LENGTH
1610
DMAC STATUS
APPLICATION DEPENDANT
1606
1612 2
APPLICATION DEPENDANT
1612 3
APPLICATION DEPENDANT
1612 1
1612 4
APPLICATION DEPENDANT
1612 5
APPLICATION DEPENDANT
DATA BUFFER
BUFFER LENGTH
1616
1602B
NEXT DESCRIPTOR POINTER
1604
BUFFER ADDRESS
1606
1608
BUFFER LENGTH
1610
DMAC STATUS
APPLICATION DEPENDANT
1612 2
APPLICATION DEPENDANT
1612 3
APPLICATION DEPENDANT
1612 1
1612 4
APPLICATION DEPENDANT
1612 5
APPLICATION DEPENDANT
1600

FIG. 16

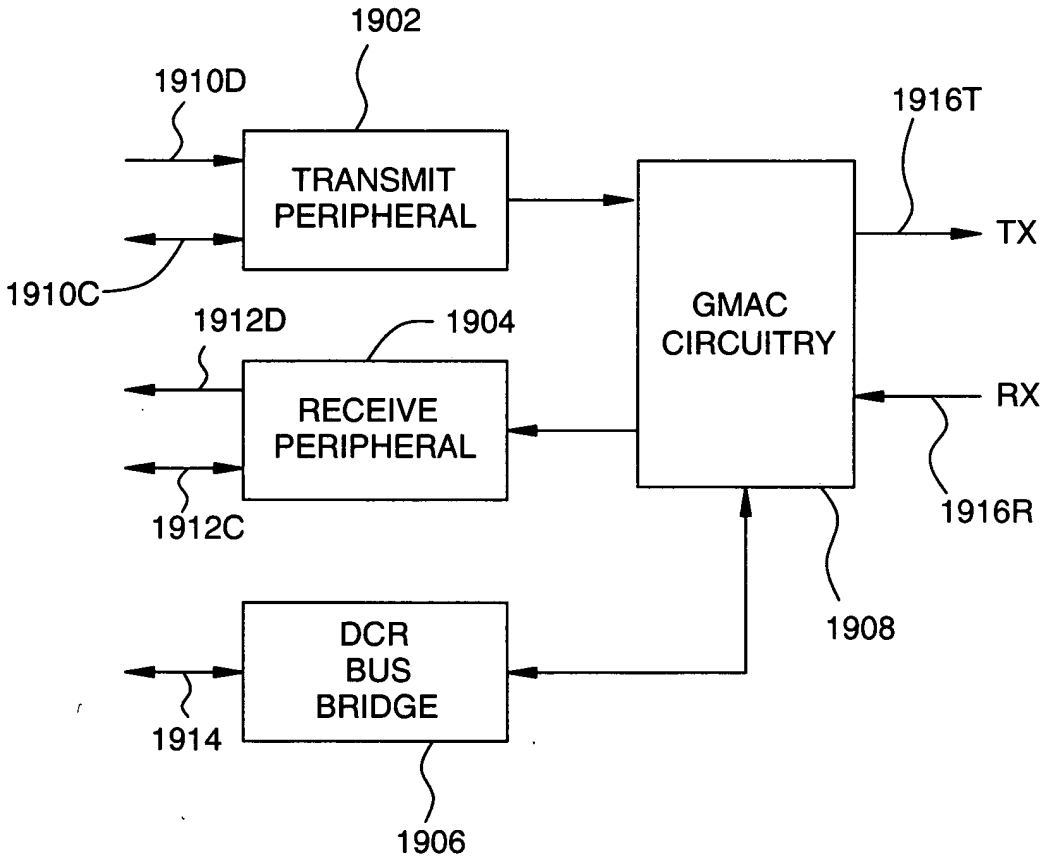

1902
1910D
TRANSMIT PERIPHERAL
1916T
TX
1910C
GMAC CIRCUITRY
1912D
1904
RECEIVE PERIPHERAL
RX
1912C
1916R
1908
DCR BUS BRIDGE
1914
1906

FIG. 19

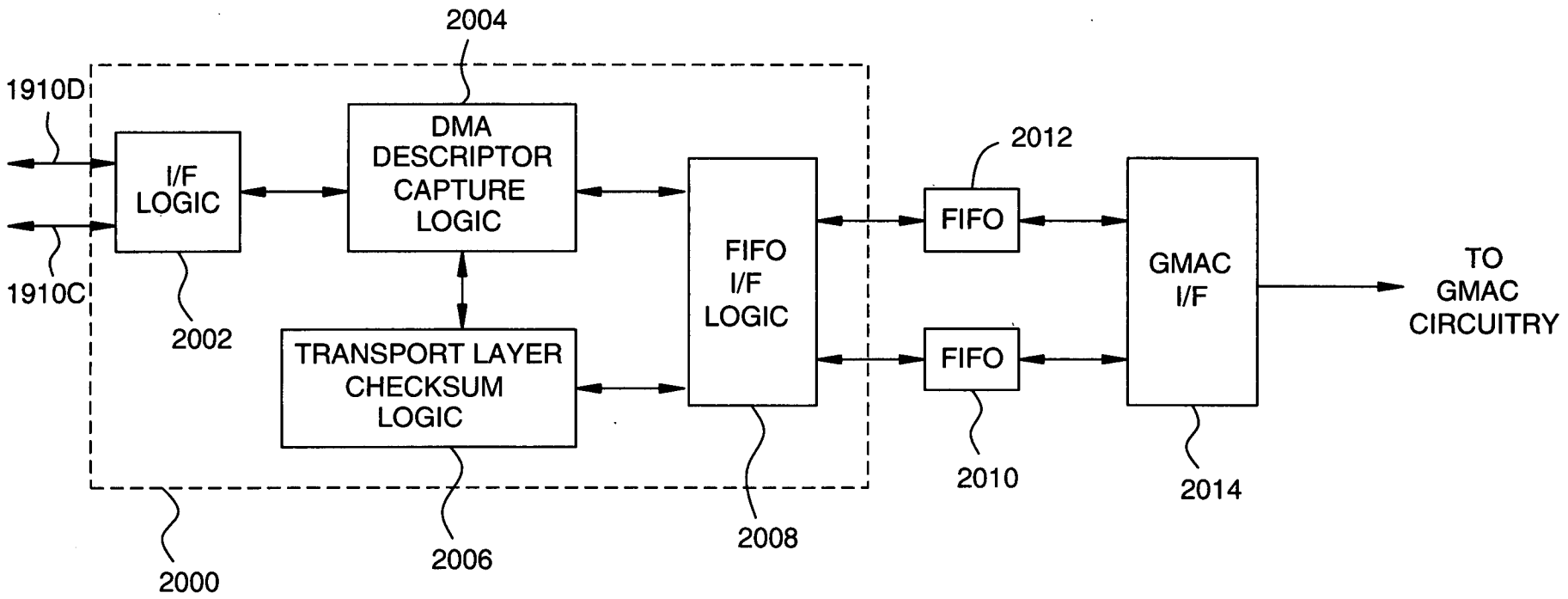

2004
1910D
I/F
LOGIC
DMA
DESCRIPTOR
CAPTURE
LOGIC
2012
FIFO
GMAC
I/F
TO
GMAC
CIRCUITRY
1910C
2002
TRANSPORT LAYER
CHECKSUM
LOGIC
FIFO
I/F
LOGIC
FIFO
2010
2014
2000
2006
2008

FIG. 20

1902

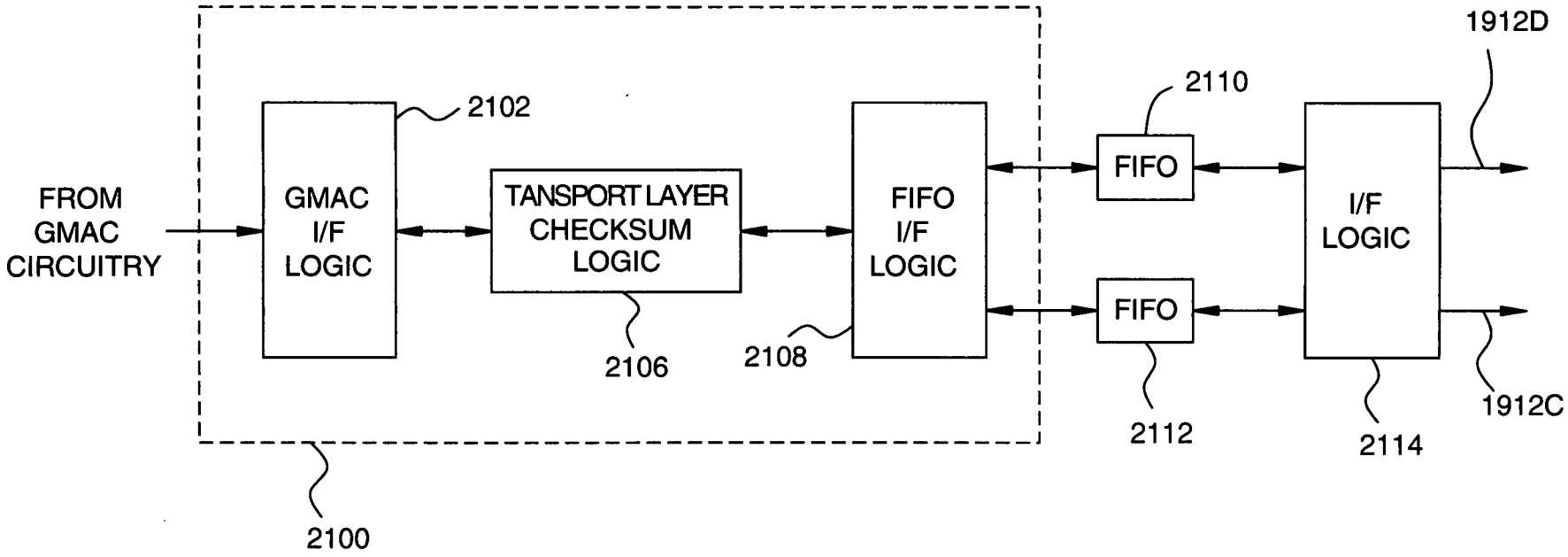

FROM GMAC CIRCUITRY
GMAC I/F LOGIC
2102
TANSPORT LAYER CHECKSUM LOGIC
2106
2108
FIFO I/F LOGIC
2110
FIFO
FIFO
2112
I/F LOGIC
2114
1912D
1912C
2100
1904

FIG. 21